IN THE CLAIMS

1. (Original) A logical connection port for an embedded device testing system, the testing system comprising apparatus adapted to compare actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs, wherein the logical connection port is adapted to indicate a predefined timing reference for determining a point in time at which to sample an output vector as the corresponding output vector in an input/output vector pair.

2. (Currently Amended) The[[A]] logical connection port ~~as claimed in~~ of claim 1 wherein the logical connection port resides in a DUT model.

3. (Currently Amended) The[[A]] logical connection port of claim 1~~as claimed in claim 1or 2~~, wherein the sampled output vector comprises a modelled vector of one or more of:

   a smoke detector;

   a fire detector;

   a security device;

   a medical device;

   a biological tissue processing device; and

   an industrial process device.

4. (Currently Amended) The[[A]] logical connection port ~~as claimed in~~ of claim 1, ~~2 or 3,~~ wherein the sampled output vector comprises an actual vector of one or more of:

a smoke detector;

a fire detector;

a security device;

a medical device;

a biological tissue processing device; and

an industrial process device.

5. (Currently Amended) The[[A]] logical connection port ~~as claimed in~~ of claim 1 ~~to 4~~ wherein the predefined timing reference may comprise one of:

one delay period being a delay period common to all input test vectors,

and;

a predetermined delay period for each input test vector.

6. (Original) A method of testing at least one embedded DUT comprising the steps of:

(a) determining a test configuration parameter set comprising predefined DUT test sequence rules;

(b) determining a first data set comprising input test vectors based on the test configuration parameter set;

(c) processing the first data set in a DUT model to determine output test vectors wherein the output test vectors comprise DUT model generated responses to the input test vectors;

(d) processing the first data set and the output test vectors to determine a second data set comprising pairs of stabilised input and output test vectors;

(e) communicating the stabilised input test vectors to at least one DUT via a DUT independent interface so that the at least one DUT is stimulated by the stabilised input test vectors to produce DUT output vectors;

(f) determining a third data set comprising the stabilised input vectors and corresponding DUT output vectors;

(g) comparing the third data set with the second data set to determine a comparison of actual behaviour to modelled behaviour of the at least one DUT.

7. (Currently Amended) The[[A]] method ~~as claimed in~~ of claim 6 wherein step d) further comprises the steps of:

(h) parsing the output test vectors with the first data set in accordance with a predefined timing reference in which the predefined timing reference determines a point in time to sample an output test vector as a stabilised output test vector;

(i) matching each stabilised output test vector to a corresponding input test vector to form pairs of stabilised input and output test vectors.

8. (Currently Amended) The[[A]] method ~~as claimed in~~ of claim 7 wherein the predefined timing reference is derived from a logical connection port as claimed in claim 1~~any one of claims 1 to 5~~.

9. (Currently Amended) The[[A]] method as claimed in claim 6~~any one of claims 6 to 8~~

wherein the DUT independent interface comprises an interprocess communication protocol utilising one of:

TCP/IP;

Active-X; and

a serial communications standard.

10. (Currently Amended) The [[A]]method ~~as claimed in any one of claims 6 to 9~~ of claim 6 wherein the DUT model comprises one or more of the following abstraction techniques:

architectural level descriptions;

data type definitions;

state transition diagrams;

extended Message Sequence Charts.

11. (Currently Amended) The[[A]] method ~~as claimed in any one of claims 6 to 10~~ of claim 6 wherein the data sets comprise test vector formatted files.

12. (Currently Amended) The[[A]] method ~~as claimed in any one of claims 6 to 11~~ of claim 6 wherein the test configuration parameter set comprises a test parameter configuration file.

13. (Currently Amended) The[[A]] method ~~as claimed in any one of claims 1 to 12~~ of claim 6 wherein the DUT comprises one or more of:

a smoke or fire detector;

a security device;

a medical device;

a biological tissue processing device;

an industrial process device.

14. (Currently Amended) Apparatus adapted to test at least one embedded device (DUT), said apparatus comprising:

processor means adapted to operate in accordance with a predetermined instruction set,

said apparatus, in conjunction with said instruction set, being adapted to perform the method steps as defined in claim 6~~any one of claims 6 to 13~~.

15. (Original) A generic test execution engine for testing at least one embedded DUT comprising:

(a) a test vector interface comprising parsing means for parsing modelled output test vectors with predefined input test vectors in accordance with a predefined timing reference to determine a test vector file comprising pairs of corresponding stabilised input and output test vectors;

(b) a DUT interface comprising addressing means for addressing, via data ports, test vectors to respective DUT's in accordance with an address identifier within the test vector file, and communication means for receiving DUT output vectors in response to the test vectors;

(c) a test result interface comprising processing means for processing respective pairs

of stabilised input and output test vectors and corresponding received DUT output vectors.

16. (Currently Amended) The[[A]] generic test execution engine ~~as claimed in~~ of claim 15 wherein the predefined timing reference is derived from a logical connection port as claimed in claim 1~~any one of claims 1 to 5~~ so as to determine a point in time to sample an output test vector in order to be determined as a stabilised output test vector for a corresponding input test vector.

17. (Currently Amended) The[[A]] generic test execution engine ~~as claimed in~~ of claim 15~~or 16~~ wherein the generic test execution engine is adapted for testing at least one DUT wherein the at least one DUT comprises one or more of:

a smoke or fire detector.

a security device;

a medical device;

an industrial process device.

18. (Currently Amended) An embedded device testing system comprising:

a generic test execution engine as claimed in claim 15~~any one of claims 15 to 17~~;

and

logging means operatively associated with the test result interface for recording an indication of a comparison between respective pairs of stabilised input and output test vectors and corresponding received DUT output vectors.

19. (Currently Amended) The[[A]] system ~~as claimed in~~ of claim 18 wherein the recorded indication comprises a formatted file comprising the following fields:

Date TimeStamp;

Evaluated Result;

A Binary String representing a logical comparison of each port value between respective test and DUT output vectors;

Port Identifier;

Port value comprising one of matched port value and expected value/actual value.

20. (Original) A data format for use in an embedded DUT testing system, the data format comprising an input test vector field correspondingly paired with an output test vector field wherein:

the input test vector field comprises predefined input information;

the output test vector field comprises predefined output information determined by sampling output information, provided in response to corresponding predefined input information, at a point in time determined by a predefined timing reference.

21. (Currently Amended) A data format ~~as claimed in~~ of claim 20 wherein the predefined timing reference is derived from the predefined input information.

22. (Currently Amended) A data format ~~as claimed in~~ of claim 20 ~~or 21~~ wherein the predefined input information comprises command set input data and the predefined

output information comprises command set output data.

23. (Currently Amended) An embedded DUT testing system data file comprising a data format as claimed in claim 20~~any one of claims 20 to 22~~.

24. (Currently Amended) A data transmission packet format for use in an embedded DUT testing system comprising a data format as claimed in claim 20~~any one of claims 20 to 22~~.

25. (Currently Amended) A computer program product comprising:

a computer usable medium having computer readable program code and computer readable system code embodied on said medium for testing at least one embedded DUT within a data processing system, said computer program product comprising:

computer readable code within said computer usable medium for performing the method of claim 6~~ steps of any one of claims 6 to 13~~.

26. (Original) A computer readable data storage medium including the computer program claimed in claim 25 stored thereon.

27. – 28. (Canceled)

29. (Original) An embedded device testing system for comparing actual device under test input/output vector pairs with modelled device under test input/output vector pairs, wherein actual device under test output vectors are sampled in accordance with a predefined timing reference.

30. (Currently Amended) The embedded device testing system ~~claimed in~~ of claim 27, wherein the predefined timing reference includes a predetermined delay period for each

one of said actual device under test input test vectors.

31. (Currently Amended) The embedded device testing system ~~claimed in~~ of claim 28, wherein the predetermined delay for each one of said actual device under test input test vectors is substantially the length of time before the corresponding output vector stabilises.

32. (Original) A process for testing an embedded device under test, including the steps of: comparing actual device under test input/output vector pairs with modelled device under test input/output vector pairs, wherein actual device under test output vectors are sampled in accordance with a predefined timing reference.

33. (Currently Amended) The process ~~claimed in~~ of claim 30, wherein the predefined timing reference includes a predetermined delay period for each one of said actual device under test input test vectors.

34. (Currently Amended) The process ~~claimed in~~ of claim 31, wherein the predetermined delay for each one of said actual device under test input test vectors is substantially the length of time before the corresponding output vector stabilises.

35. (Original) Apparatus for testing a device under test, including:

(a) means for applying a test input vector to the device under test; and

(b) means for sampling an output vector from the device under test in response to said input vector,

wherein the wherein said sampling is effected in accordance with a predefined timing

reference.

36. (Currently Amended) The apparatus ~~claimed in~~ of claim 35, wherein the predefined timing reference includes a predetermined delay period.

37. (Currently Amended) The apparatus ~~claimed in~~ of claim 34, wherein the predetermined delay is substantially the length of time before the corresponding output vector stabilises.

38. (Previously Presented) A logical connection port for an embedded device testing system, the testing system comprising apparatus adapted to compare actual device under test (DUT) input/output vector pairs with modelled DUT input/output vector pairs, wherein the logical connection port is adapted to indicate a predefined timing reference for determining a point in time at which to sample an output vector as the corresponding output vector in an input/output vector pair;

wherein the logical connection port resides in a DUT model;

wherein the sampled output vector comprises an actual vector of one or more of:

a smoke detector;

a fire detector;

a security device;

a medical device;

a biological tissue processing device; and

an industrial process device; and

wherein the predefined timing reference may comprise one of:

one delay period being a delay period common to all input test vectors, and;

a predetermined delay period for each input test vector.